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Numerical Modeling of Cyclic Stress-strain Behavior of Sn-Pb Solder Joint During Thermal Fatigue

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ABSTRACT

This study examines the cyclic stress-strain response of solder joints in a surface mounted electronic assembly due to temperature cycles. For this purpose, a three dimensional model of an electronic test package is analyzed using finite element method. The model consists of 92 solder joints arranged along the peripheral of a 24 x 24 solder array. The various different materials considered in the simulation are Si-die, 60Sn-40Pb solder alloy, Cu-traces, Cu_6Sn_5 intermetallics, FR-4 substrate and printed circuit board (PCB). The temperature and strain rate dependent plastic stress-strain curves define the viscoplastic response of the near-eutectic solder alloys. Orthotropic behavior of the FR-4 substrate and PCB is modeled. Other materials are assumed to behave elastically with temperature dependent material properties. Temperature loading of the package consists of an initial cooling down from the re-flow temperature at 183 °C to 25 °C followed by thermal cycling between -40 °C to 125 °C. Results of the analysis showed that the package warps with a magnitude of 93 μm at 25 °C after re-flow. In this process, the critical solder joint accumulated an inelastic strain of 0.856 percent. Faster temperature ramp rate at 370 °C /min (load case TR1) versus 33 °C /min (load case TC1) resulted in 12 percent lower inelastic strain after completing 3 temperature cycles. However, the inelastic strain magnitude is achieved in a much shorter time. The shear stress-strain hysteresis loops display the largest strain ranges compared to other stress-strain components. The calculated shear strain range is 0.8 percent with the corresponding stress range of 34.0 MPa.

Keywords: Electronic packaging, solder joint, reliability, re-flow, cyclic stress-strain behavior, finite element method.

ABSTRAK

Kajian ini meneliti sambutan tegasan-terikan berkitar sambungan pateri dalam pemasangan elektronik pada permukaan disebabkan oleh kitaran suhu. Untuk tujuan ini, suatu model pakej ujian elektronik tiga dimensi dianalisis menggunakan kaedah unsur terhingga. Model ini mengandungi 92 sambungan pateri yang disusun di sepanjang persisian 24 x 24 tatasusunan pateri. Pelbagai jenis bahan yang diambil kira dalam simulasi ini ialah dai-Si, aloi pateri 60Sn-40Pb, pengesan-Cu, antaralogam Cu_6Sn_5*, lapisan FR-4 dan papan*

litar tercetak (PCB). Lengkung tegasan-terikan plastik yang bergantung kepada suhu dan kadar terikan menjelaskan sambutan likatplastik aloi pateri hampir-eutektik ini. Kelakuan ortotrop lapisan FR-4 dan PCB juga dimodelkan. Bahan-bahan lain dianggap bersifat elastik dengan sifat bahan yang bergantung kepada suhu. Pembebanan suhu pakej terdiri dari penyejukan permulaan daripada suhu alir-semula pada 183 °C ke 25 °C diikuti oleh kitaran terma di antara –40 °C ke 125 °C. Keputusan analisis menunjukkan yang pakej tersebut melengkung sebesar 93 μm pada suhu 25 °C selepas aliran semula. Dalam proses ini, sambungan pateri yang kritikal mengumpul terikan tak-elastik sebanyak 0.856 peratus. Kadar tanjakan suhu lebih pantas pada 370 °C/min (kes beban TR1) berbanding 33 °C/min (kes beban TC1) menghasilkan terikan tak-elastik 12 peratus lebih rendah selepas selesai 3 kitar suhu. Walau bagaimanapun, magnitud terikan tak-elastik diperolehi dalam masa yang lebih pantas. Gelung histerisis tegasan-terikan ricih menunjukkan julat terikan terbesar berbanding komponen tegasan-terikan yang lain. Julat terikan ricih yang dikira ialah 0.8 peratus pada julat tegasan 34.0 MPa.

Kata kunci: Pakej elektronik, sambungan pateri, keboleharapan, alir-semula, kelakuan tegasan-terikan kitar, kaedah unsur terhingga.

INTRODUCTION

In a surface mount electronic assembly, the electronic package is commonly attached to the printed circuit board (PCB) by solder joints. Temperature fluctuation due to device internal heat dissipation and ambient temperature changes generates thermo-mechanical loading on the assembly. Throughout the loading, differential thermal expansion of the various component materials induces cyclic strains on the solder joints. These strains result in cumulative fatigue damage that could lead to premature fatigue failure of the joints. Thermal fatigue of solder joints, therefore, is critical to electronic package performance and reliability. The reliability of these solder joints is determined by the combined effects of component design, assembly design and use environment.

Temperature cycling of solder assemblies in an environmental chamber is intended to duplicate the characteristics of the actual operating (power) cycles that consist of power on/off with or without ambient temperature changes. In this thermal cycling, the solder joint is subjected to cyclic stresses and strains. The observed strain level exceeded the elastic limit of the solder alloy (Pang et al. 1998, Amagai 1999, Yeo et al. 2002, Zhai et al. 2003). Consequently, the stress-strain hysteresis loops dictate the accumulation of fatigue damage and determine the fatigue life of the solder joint. The low cycle fatigue (LCF) failure mechanism is complicated by the creep-fatigue interaction effect since the solder joint operates at high homologous temperature. At this temperature level, the solder alloy display significant rate dependent behavior (Adams 1986, Pang et al. 1998, Sasaki et al. 2001).

Finite element modeling of electronic packages and PCB assembly has been widely employed to provide an insight to the understanding of failure mechanisms and long-term reliability of solder joints in the assemblies (Lau 1995, Lau and Yi-Hsin 1997). Numerous models, however do not account for residual stress and strain states in the solder joints resulting from solder re-flow process (Lau 1996, Amagai 1999, Gustafsson et al. 2000, Shi et al. 2000, Pang et al. 2001, Yeo et al. 2002, Zhai et al. 2003, Lee et al. 2004, Ridout et al. 2004). Finite element modeling success lies in appropriate representation of the package geometry with associated boundary conditions and temperature loading, and the ability to accurately simulate the response of package materials during thermal cycling or shock. Consequently, an accurate description of solder alloy behavior should account for both temperature and time-rate effects on the material as observed experimentally (Adams 1986). For example, the tensile strength of eutectic Sn-Pb solder decreases from about 50 to 30 MPa following 60 days of thermal aging (Kishimoto et al. 2001). In addition, solder tensile properties can vary widely for different strain rates used in the tensile tests (Pang et al. 1998).

This paper investigates the cyclic stress-strain response of Sn-Pb solder joints connecting a test package to the PCB during re-flow and subsequent thermal cycles. The package responses to thermal cycles without considering the solder re-flow process are modeled for comparative study. Emphasis will be placed on the evolution characteristics and hysteresis cycles of stresses and strains, in relation to LCF failure of the solder joint. The relative effects

of temperature ramp rates on the deformation response of the package are examined in terms of inelastic strain accumulation in the solder alloy.

FINITE ELEMENT MODELING

The finite element model of the test package consists of 92 solder joints arranged along the peripheral of a 24 x 24 solder array. The diameter, height and pitch distance of the solders is 750 μm, 600 μm and 1.0 mm, respectively. Due to symmetrical nature of the package, only one-quarter of the 3D model is analyzed as illustrated in Figure 1. Geometrical boundary conditions for planes of symmetry are imposed on the model. All surfaces are assumed perfectly bonded at contact surfaces. The various different materials considered in the simulation are Si-die, near eutectic solder joints, Cu-traces, Cu_6Sn_5 intermetallics, FR-4 substrate and PCB. Thermal analysis performed on the test package indicated that the transient effect is negligible, thus thermal boundary condition was not imposed in the stress analysis.

Temperature dependent material properties of Si, solder alloy, Cu-traces and FR-4 employed in the analysis are extracted from these papers (Adams 1986, Auersperg 1997, Amagai 1999, Pang et al. 2002). Orthotropic behavior of the FR-4 substrate and PCB was modeled. Summary of the materials properties used in the simulation is shown in Table 1. Strain-rate-dependent plastic stress-strain curves define the viscoplastic response of the 60Sn-40Pb solder alloys. The stress-strain curves of the solder alloy at several test temperatures in the range of –40 to 125 °C and at three different straining rates were considered. An example of the stress-strain responses is reproduced in Figure 2 (Adams 1986).

Thermal loading of the test package, as illustrated in Figure 3, consists of an initial cooling down from the re-flow temperature (183 °C) to room temperature, followed by thermal cycling between –40 to 125 °C (TC1). The effect of high temperature ramp rate (to simulate thermal shock stress) is examined by comparing two different cases at 33 °C/min (TC1) and 370 °C/min (TR1). Thermal cycles identical to TC1 but without considering the re-flow process (TC0) is also modeled.

RESULTS AND DISCUSSION

Re-flow Process (Cool-down)

Results of the finite element analysis show that the test package warps downward (with PCB on the bottom side) at room temperature (25 °C) following the re-flow process as shown in Figure 4. The maximum calculated warpage (vertical displacement) is 93 μm. The typical magnitude of warpage observed for chip scale package (CSP) was 112 μm at the room temperature (Lee et al. 1998).

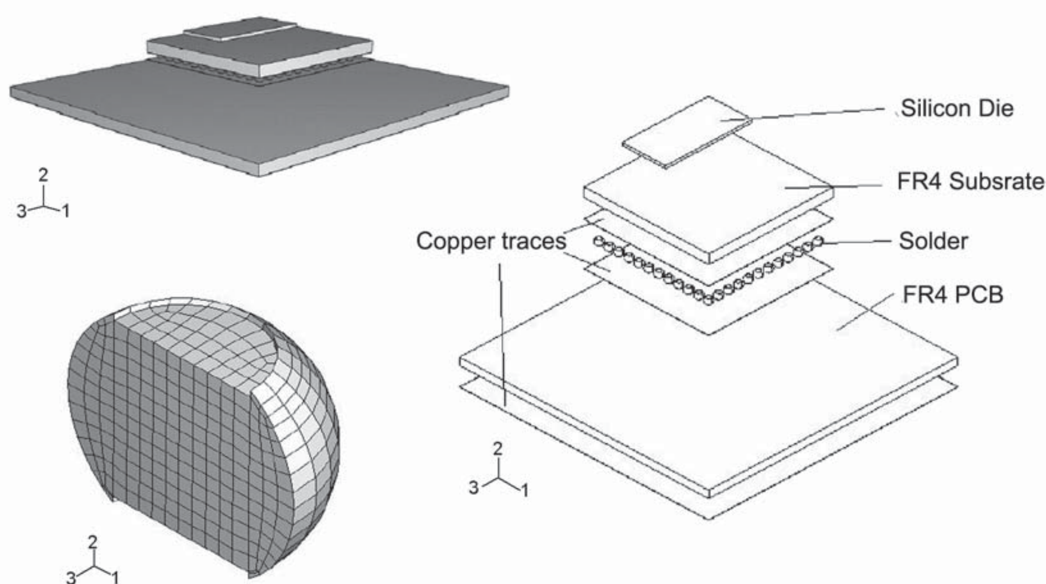


FIGURE 1. Isometric and exploded view of the test package (quarter model). The inset figure illustrates mesh size for the cross- section view of a solder joint

TABLE 1. Properties of the various materials used in the simulation: Young's modulus (E), poison ratio (*V*), coefficient of thermal expansion (α), and shear modulus (G)

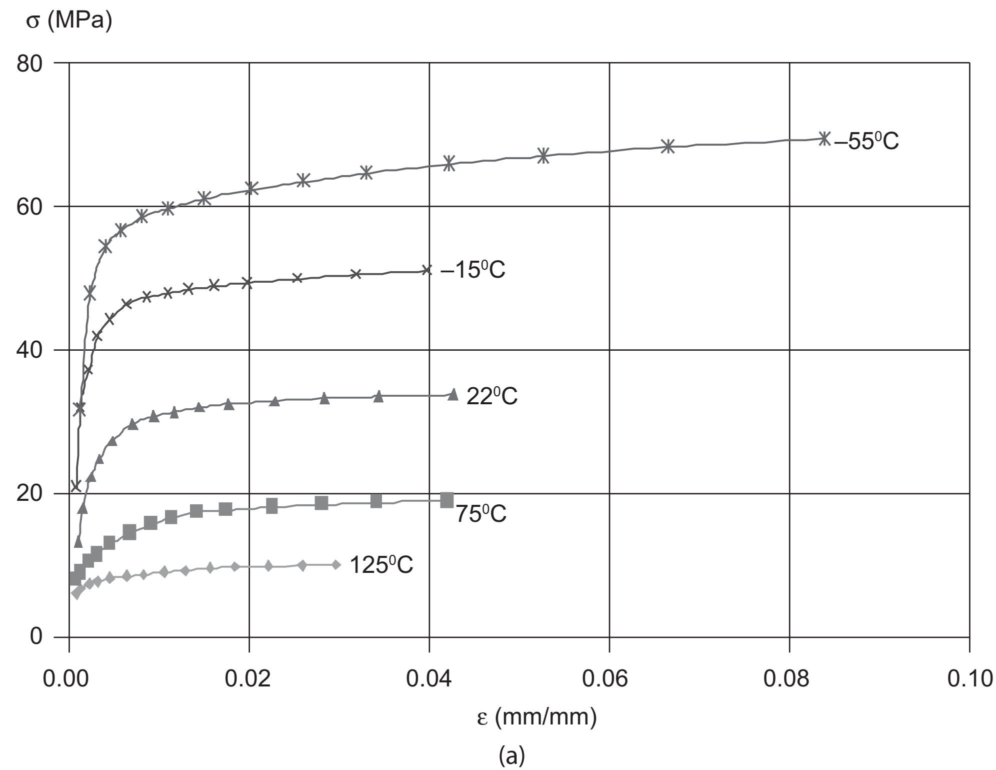
Material	Modulus of Elasticity, E (GPa) *T* in Kelvin	Poisson's Ratio, *v* *T* in Kelvin	CTE, α (ppm/K) *T* in Kelvin
60Sn 40Pb (Adams, 1986)	64.26 – 0.0718 * *T*	$0.3244 + 1.1558 \times 10^{-4} * T$	21
Silicon (Shi *et al.*, 2002)	132.46 – 0.00954 *T*	0.28	2.113 + 0.00235 *T*
Copper (Shi *et al.*, 2002)	141.92 – 0.0442 *T*	0.35	15.64 + 0.0041 *T*
IMC CU_6SN_5 (Amagai, 1999a)	85.6	16.0	0.31

FR-4 (isotropic plane xy) (Auersperg, 1997)

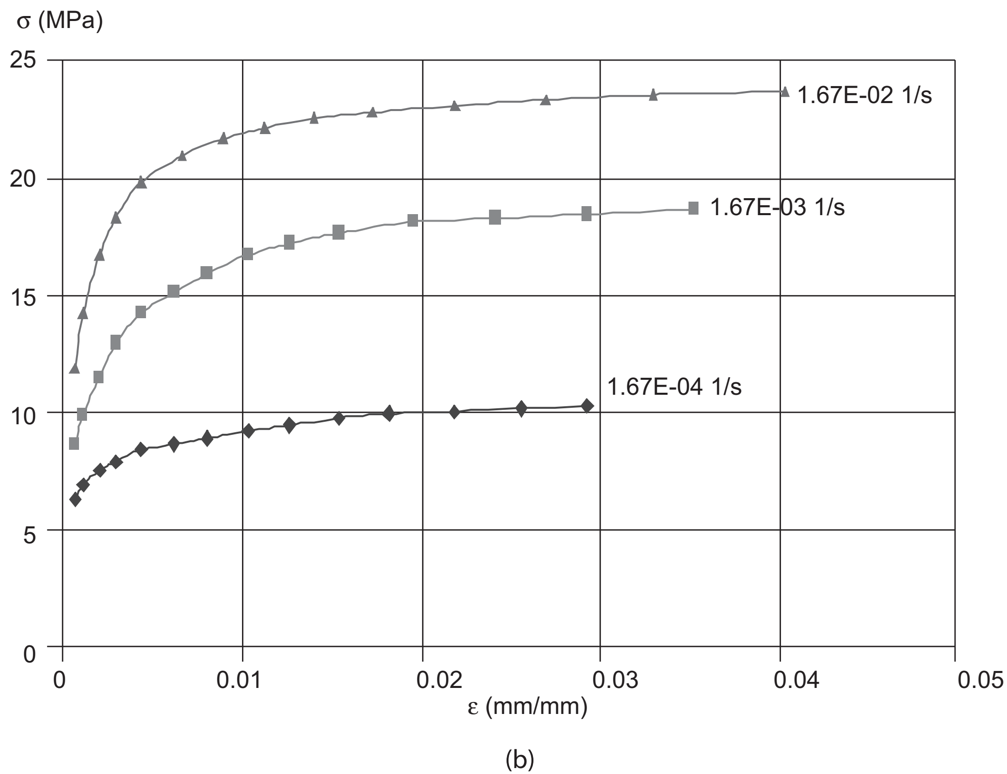
Properties	-40°C	30°C	95°C	125°C	150°C	270°C
Ex (MPa)	24252	22400	20680	19300	17920	16000
Ey (MPa)	24252	22400	20680	19300	17920	16000
Ez (MPa)	2031	1600	1200	1000	600	450
V_{xy}	0.02	0.02	0.02	0.02	0.02	0.02
V_{yz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
V_{xz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
α_x(ppm/°C)	16	16	16	16	16	16
α_y(ppm/°C)	16	16	16	16	16	16
α_z(ppm/°C)	65	65	65	65	65	65
Gxy (MPa)	662	630	600	500	450	441
Gxz (MPa)	210	199	189	167	142	139
Gyz (MPa)	210	199	189	167	142	139

The solder joint located at the symmetry line that is parallel to the longer side of the Si-die is the most critically strained solder (marked A in Figure 4). The evolution of von Mises stresses and the corresponding equivalent inelastic strains in this critical solder joint throughout the re-flow process is illustrated in Figure 5. It is noted that inelastic strains developed early following cooling down of the package from 183 °C to 25 °C during the re-flow process. Although the stress level induced by coefficient of thermal expansion (CTE) mismatch is low, the yield strength of the solder was also relatively low at high temperature. In addition, at this high homologous temperature, creep strain rate of the solder alloy is significant and contributes to inelastic strain. The typical yield strength of 60Sn-40Pb solder alloys was 8 MPa at 125 °C when strained at 1.67×10^{-4} per second (Adams 1986). At higher temperature up to 183 °C the yield strength of the solder alloy was expected to continuously decrease. The stress is brought to the yield surface with the continuously accumulated inelastic strains. The von Mises stress reaches 24.0 MPa with the corresponding inelastic strain of 0.856 percent at the room temperature.

In the critical solder joint, a high stress gradient developed along the interface between the solder and the Cu_6Sn_5 intermetallic owing to both thermal expansion mismatches between the two materials and the severe geometric discontinuities. The typical calculated von Mises stress and the corresponding equivalent inelastic strain distribution in the critical solder at 25 °C is shown in Figure 6. It is worth noting that the region of high stress occurs only to a small depth from the surface of the solder while the bulk of the solder remains elastic. The location underneath the edges of the substrate (or intermetallic phase) is experiencing the maximum stress and strain hysteresis during subsequent thermal cycles. Needle-like structures and Kirkendal voids have



(a)



(b)

FIGURE 2. Stress-strain behavior of 60Sn-40Pb solder alloy (a) at a constant strain rate of 1.67×10^{-4} s^{-1} and (b) at a constant temperature of 125 °C (Adams 1986)

been observed at the Cu_6Sn_5 intermetallics and solder joint. These material features contribute to localized stress concentration. Consequently, extensive accumulation of cyclic inelastic strains in this locality is likely to initiate the fatigue crack along the solder /intermetallic interfaces. Crack initiation in the solder corresponds to the location of the maximum creep and plastic strain (Sarihan 1999). In addition, solder fatigue cracking has been observed to initiate and propagate

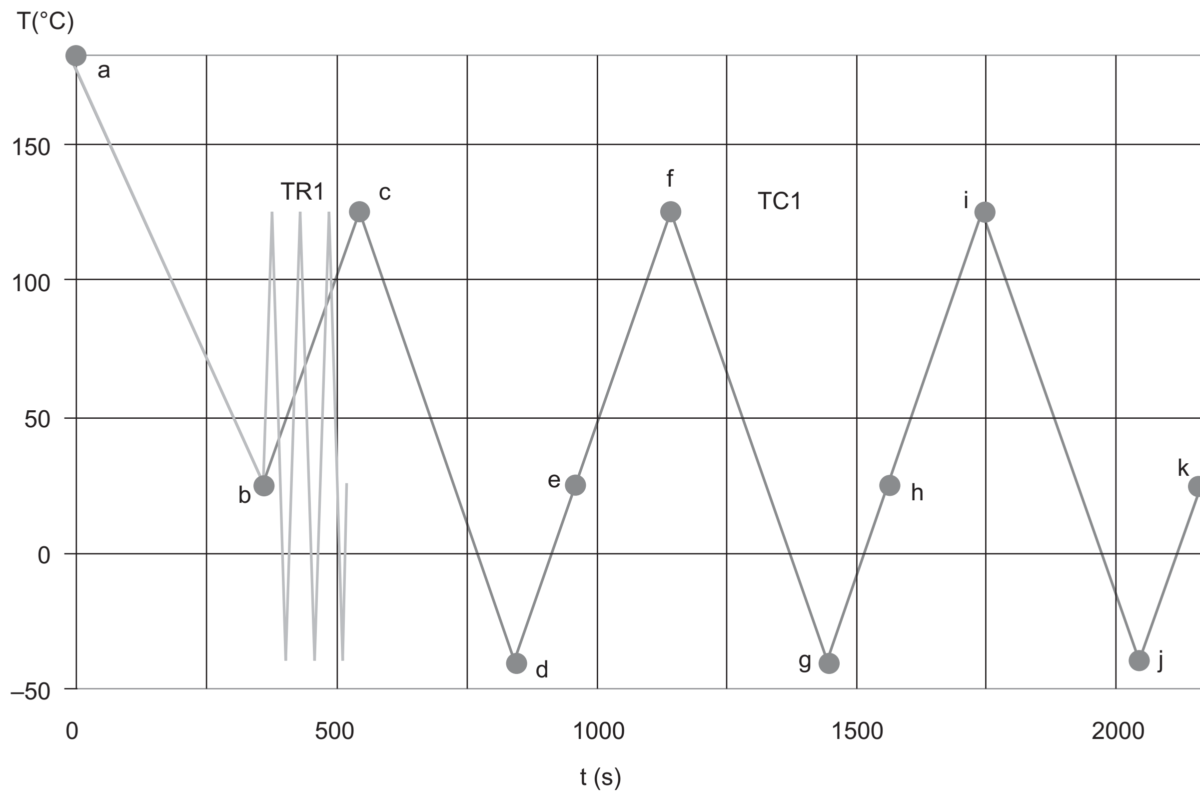


FIGURE 3. Temperature-time loading profile consists of re-flow process (path a-b) followed by temperature cycles

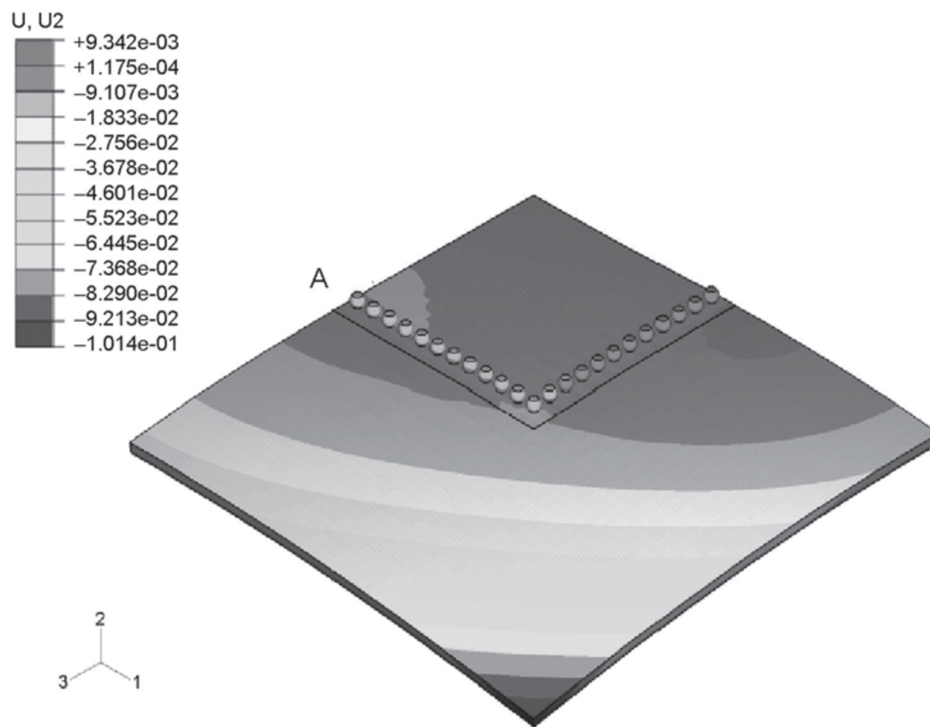


FIGURE 4. Calculated warpage of the test package at 25 °C following solder re-flow process. The top substrate and Si-die layers are not shown

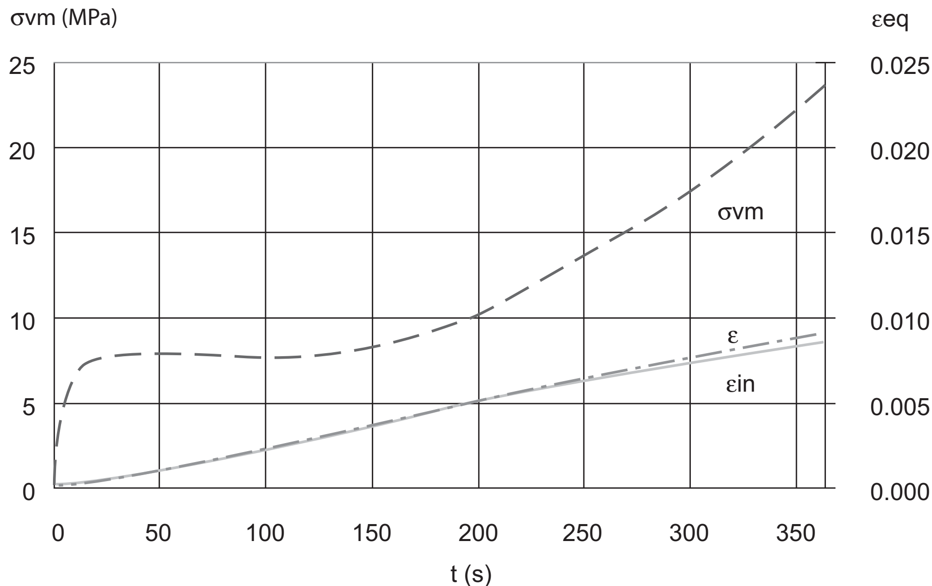


FIGURE 5. Evolution of von Mises stresses, equivalent total and inelastic strains in the critical solder during re-flow process

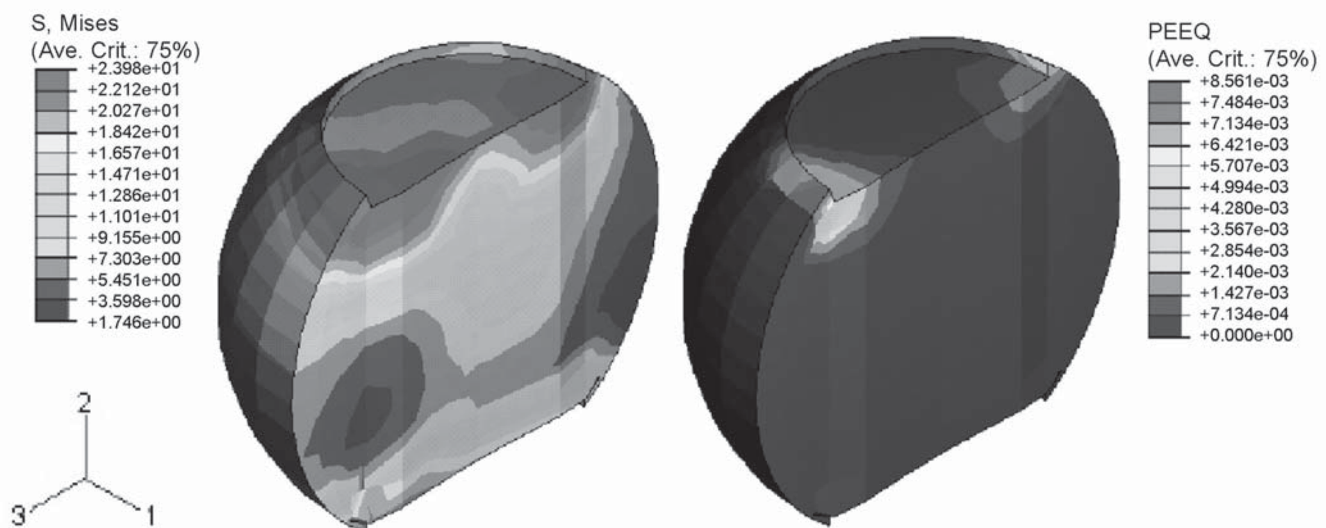


FIGURE 6. von Mises stress and inelastic strain distribution in the critical solder joint at 25°C following re-flow process (cross-sectional view)

from similar location in chip scale packages (Lee et al. 1998 and Amagai 1999). Catastrophic propagation of such crack is governed by fatigue and fracture parameters including stress level, fracture toughness and threshold stress intensity factor range.

THERMAL CYCLES

The evolution characteristics of internal states in the critical solder joint during the application of temperature cycles are examined. Figure 7 compares the predicted inelastic strains in the critical solder joint for the two different heating and cooling rates. The heating and cooling rates for load case TR1 is 11.2 times faster than for load case TC1. Results showed that the accumulated inelastic strain for load case TR1 after completing 3 thermal cycles is about 12 percent lower than that for load case TC1. The accumulation of inelastic strain in thermal shock cycles (TR1) was primarily due to the fatigue effect whereas in the slow temperature cycles (TC1) longer time is spent at higher stress, where fatigue and creep occur simultaneously resulting in greater inelastic (creep) strain per cycle. However, the inelastic strain magnitude was achieved in much

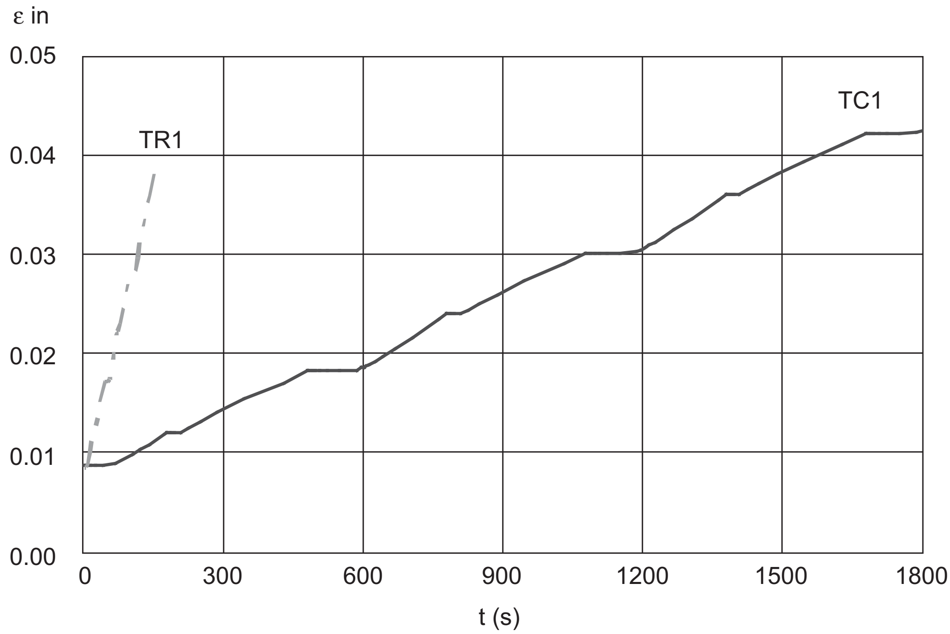


FIGURE 7. Effect of temperature ramp rates on the evolution of inelastic strain in the critical solder joint after completing 3 thermal cycles

shorter time for thermal shock cycling (TR1). This result demonstrates the feasibility of employing thermal shock cycling as an alternative to temperature cycling in a reliability analysis on electronic packages for faster data turnaround.

The stress-strain hysteresis response of the solder alloy was examined in view of the fatigue life prediction of solder joint. Figure 8 shows the hysteresis loops for all cartesian components of stresses and strains in the critical solder joint. The

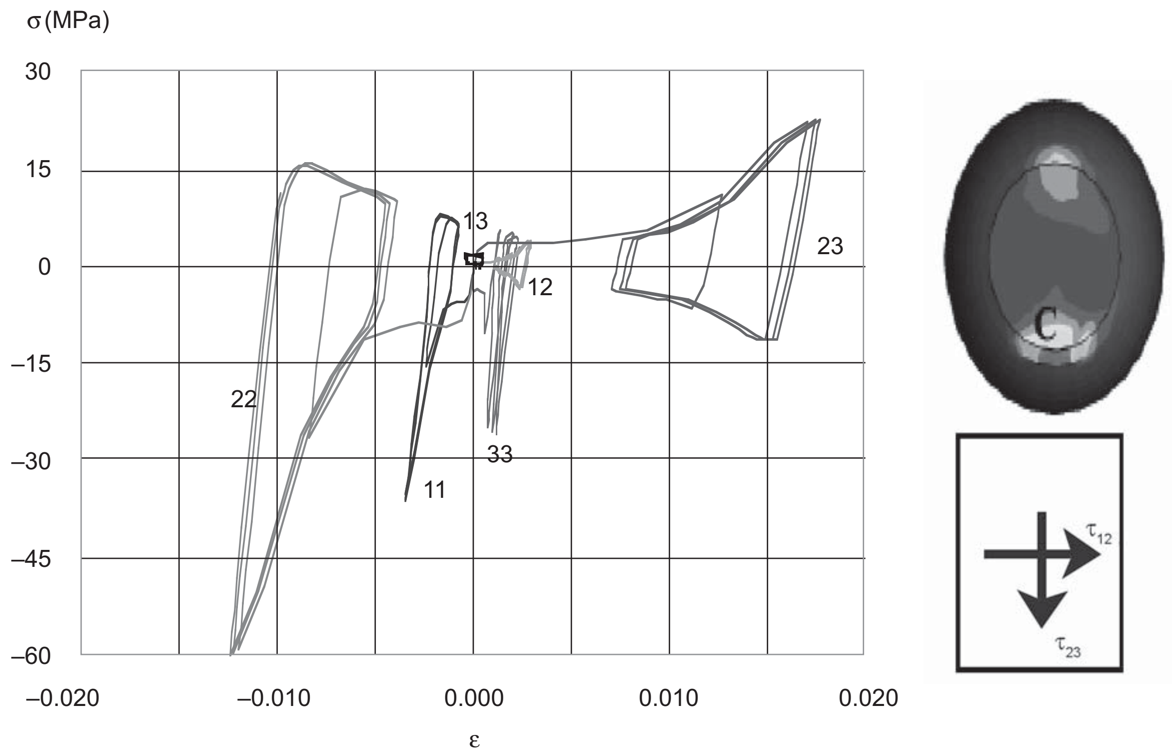


FIGURE 8. Stress-strain hysteresis loops at the critical point C for the first three temperature cycles of load case TC1. The indices denote the six cartesian components. τ_{12} and τ_{23} indicate directions of shear stresses on the stressed element

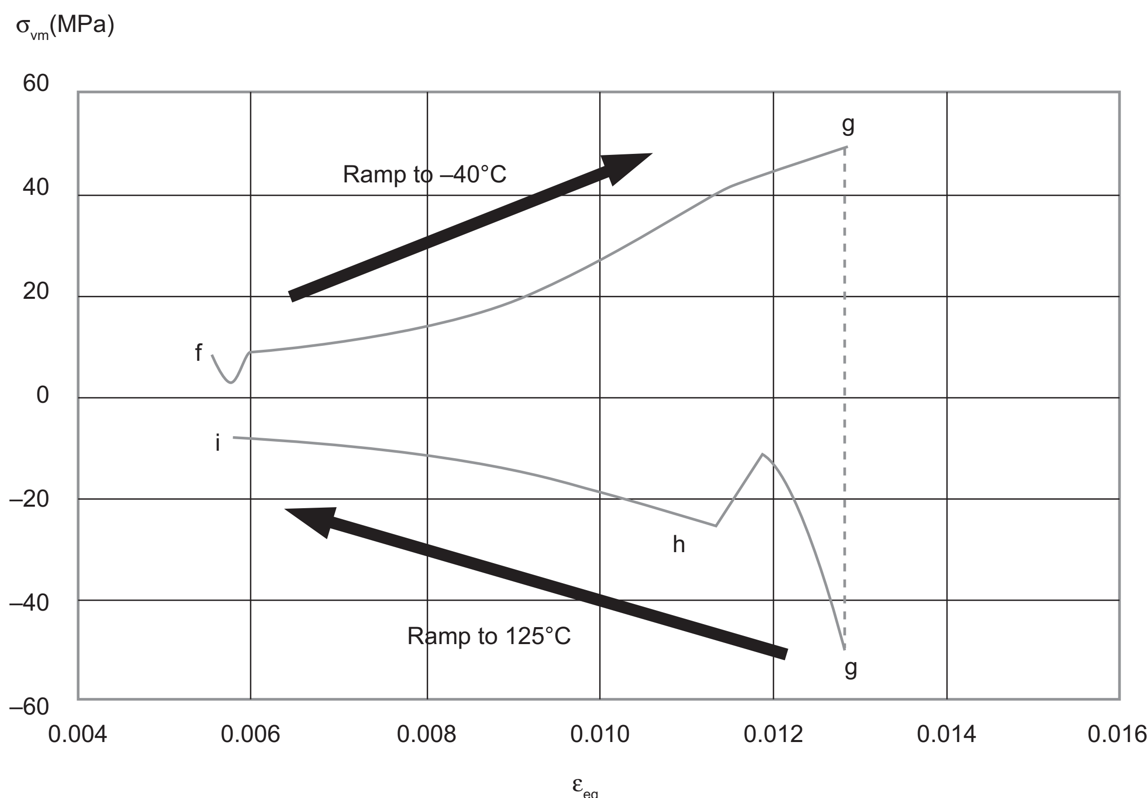


FIGURE 9. Equivalent stress-strain hysteresis loop for the 2nd thermal cycle following solder re-flow process

largest stress range was observed for the tensile component (22-direction) with a magnitude of 78 MPa. The tensile part of this stress was favorable to Mode-I crack initiation at the solder/ intermetallic interface layer. The shear strain component (23-direction) displays the largest strain range (at zero stress) of 0.8 percent with the corresponding shear stress range of 34.0 MPa. This large relative displacement within the solder / intermetallic interface attenuates the cyclic interfacial shear stress and strains resulting in crack initiation, as often observed experimentally. It is noted that although the shear stress range is larger (41.0 MPa) for faster temperature ramp rate (TR1), the resulting shear strain range is similar at 0.8 percent. For comparative purpose, a typical fatigue life of eutectic solder (with cycling frequency of 10 mins./cycle) at a plastic strain range of 1.0 percent was about 5000 cycles (Hua et al. 1998). The hysteresis loop shifted towards larger strain values following each temperature cycle indicating the continuous accumulation of inelastic strain.

The combined response of all cartesian cyclic stress and strain components is examined by plotting the hysteresis loop in terms of von Mises stress and equivalent strain. Figure 9 shows the hysteresis curve for the 2nd temperature cycle between -40 and 125 °C following the re-flow process (path f-g-h-i in Figure 3). In this figure, the sign of von Mises stress is assigned to be positive for decreasing temperature and negative for increasing temperature. The finite element results show that the stress and equivalent strain in the solder increase (50.2 MPa, 1.28 %) when the temperature is decreased from 125 to -40 °C (portion f-g). When the temperature is subsequently increased the stress relaxed to 8.5 MPa while the corresponding equivalent strain decreased to 0.056 % (portion g-h-i). It is noted that during the heating process between -40 to 25 °C (path g-h), the stress components changed the sign, which is reflected in the inflection point along the hysteresis curve. This is the effect of bending induced by the warpage of the package.

THERMAL CYCLES WITHOUT SOLDER RE-FLOW PROCESS

When the solder re-flow process is not considered in modeling, the process-induced residual stress and strain are neglected at the beginning of temperature cycles. The predicted evolution

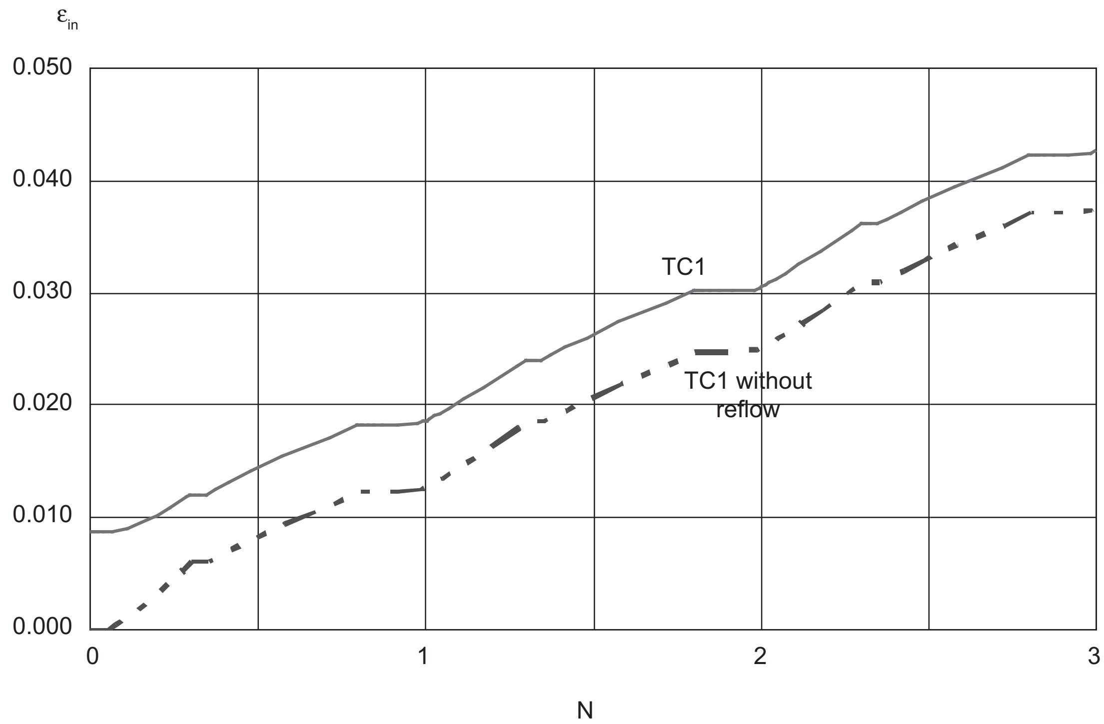


FIGURE 10. The effect of re-flow to the evolution of inelastic strain accumulation in the critical solder joint

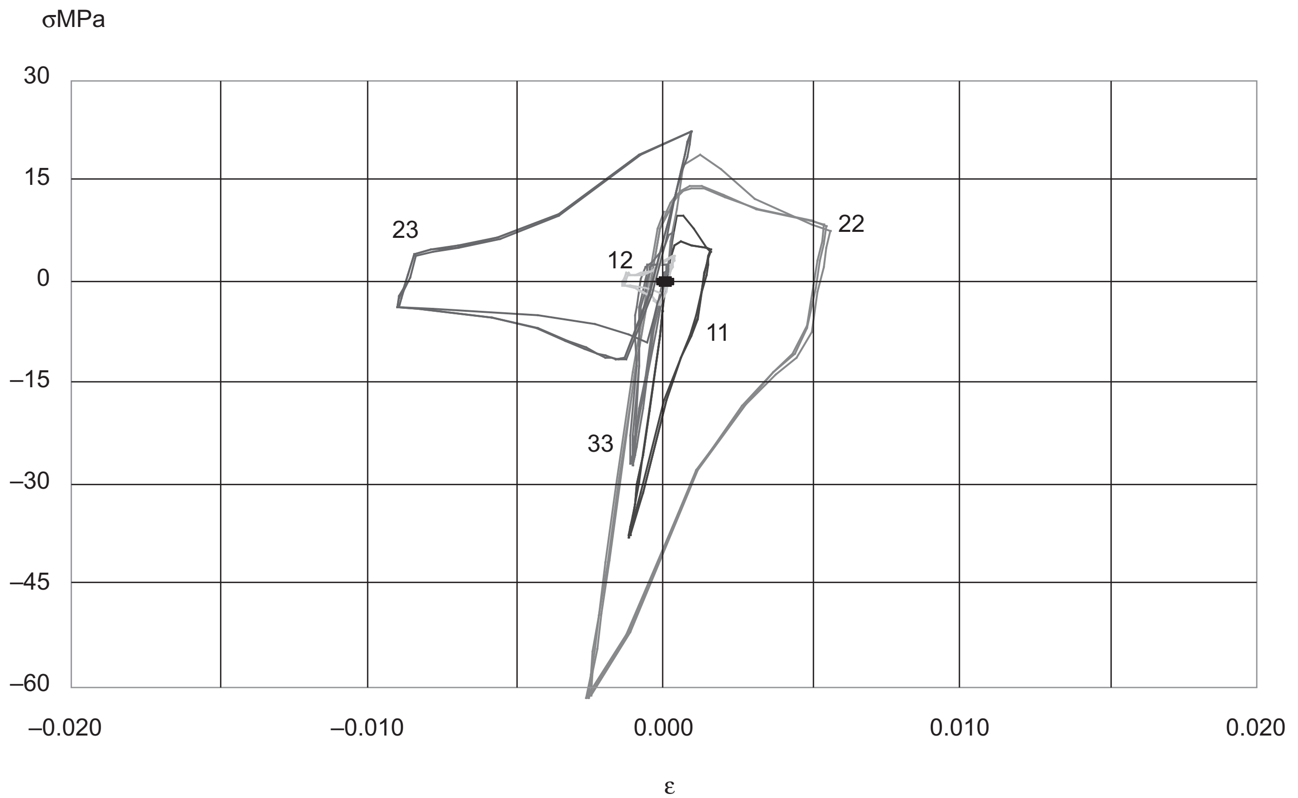


FIGURE 11. Stress-strain hysteresis plots for the first three temperature cycles of load case TC0 (without re-flow)

characteristics of inelastic strain in the critical solder joint during thermal fatigue (TC0) are shown in Figure 10. Similar trends of stress evolution and the corresponding inelastic strain accumulation with load case TC1 suggested similar damage mechanisms. The effect of re-flow residual strain on subsequent cyclic inelastic strain accumulation diminishes with applied temperature cycles. The difference between inelastic strain level for the two load cases TC1 and TC0 (no re-flow) decreases from 0.897% at the beginning of fatigue cycle to 0.479% after accumulating three cycles. The constant difference in the accumulated inelastic strains between these load cases indicated that the re-flow process had little influence on the evolution characteristics of cyclic strain in the solder joint.

Figure 11 shows the stress-strain hysteresis plots for the six cartesian components. It is noted that the size of hysteresis loops are similar to those predicted for load case TC1 (Figure 8). It follows that the predicted fatigue lives of the solder joints, based on cyclic shear strain range, were less affected by the residual internal states due to the solder re-flow. However, the mean strain level will be underestimated when the effect of solder re-flow process is not modeled.

CONCLUSIONS

The cyclic stress-strain behavior of the Sn-Pb solder joint in a surface mount test package has been analyzed using finite element analysis. Results show that:

1. The package warps downwards at 25 °C following the re-flow process with a magnitude of 93 µm. The induced inelastic strain is 0.856 percent. Additional inelastic strain of 3.5 percent is accumulated after 3 temperature cycles between -40 to 125 °C.
2. Faster temperature ramp rate (370 versus 33°C/min) accelerates the inelastic strain evolution per temperature cycle. However, the strain magnitude is 12 percent lower after 3 cycles.
3. The stress-strain hysteresis curves show the largest normal component (22-direction) of the stress range with magnitude of 78 MPa. The shear component (23-direction) of the hysteresis loops displayed the largest strain range at 0.8 percent.
4. The effect of residual stresses and strains due to solder re-flow on the accumulation of inelastic strain diminishes with increasing number of temperature cycles. Cyclic strain range is similar for both simulations, with and without considering solder re-flow process. However, the mean strain level was underestimated when modeling without considering solder re-flow process.

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