Sains Malaysiana 43(2)(2014): 267–272

Nanoscale Patterning by AFM Lithography and its Application on the Fabrication of Silicon Nanowire Devices

(Pencorakan Berskala Nano dengan Litografi AFM dan Aplikasinya dalam Fabrikasi Peranti Nanowayar Silikon)

SABAR D. HUTAGALUNG*, KAM CHUNG LEW & TEGUH DARSONO

ABSTRACT

Many techniques have been applied to fabricate nanostructures via top-down approach such as electron beam lithography. However, most of the techniques are very complicated and involves many process steps, high cost operation as well as the use of hazardous chemicals. Meanwhile, atomic force microscopy (AFM) lithography is a simple technique which is considered maskless and involves only an average cost and less complexity. In AFM lithography, the movement of a probe tip can be controlled to create nanoscale patterns on sample surface. For silicon nanowire (SiNW) fabrication, a conductive tip was operated in non-contact AFM mode to grow nanoscale oxide patterns on silicon-on-insulator (SOI) wafer surface based on local anodic oxidation (LAO) mechanism. The patterned structure was etched through two steps of wet etching processes. First, the TMAH was used as the etchant solution for Si removing. In the second step, diluted HF was used to remove oxide mask in order to produce a completed SiNW based devices. A SiNW based device which is formed by a nanowire channel, source and drain pads with lateral gate structures can be fabricated by well controlling the lithography process (applied tip voltage and writing speed) as well as the etching processes.

Keywords: AFM lithography; nanodevices; nanoscale pattern; silicon nanowire

ABSTRAK

Pelbagai teknik telah digunakan untuk fabrikasi nanostruktur melalui pendekatan atas-bawah seperti litografi alur elektron. Walau bagaimanapun, teknik tersebut sangat rumit dan prosesnya memerlukan banyak langkah, kos operasi tinggi dan menggunakan bahan kimia merbahaya. Manakala, litografi mikroskop daya atom (AFM) merupakan suatu teknik yang mudah serta dapat dikatakan tanpa topeng, melibatkan kos sederhana dan prosesnya tidak rumit. Dalam litografi AFM, pergerakan tip penduga dapat dikawal untuk menghasilkan corak berskala nano pada permukaan sampel. Bagi fabrikasi nanowayar silikon (SiNW), sebatang tip konduktif dioperasikan dalam mod AFM tak-sentuh untuk menumbuhkan corak oksida berskala nano pada permukaan wafer silikon-di atas-penebat (SOI) berdasarkan mekanisme pengoksidaan anod setempat (LAO). Struktur tercorak kemudian dipunar melalui dua langkah proses punaran basah. Pertama, TMAH telah digunakan sebagai larutan punar bagi menghilangkan Si. Langkah kedua, HF yang dicairkan digunakan menghilangkan topeng oksida untuk menghasilkan satu peranti lengkap berasaskan SiNW. Struktur peranti SiNW yang terdiri daripada suatu saluran nanowayar, pad sumber dan longkang dengan get sisi dapat dihasilkan apabila proses litografi (voltan yang dikenakan pada tip dan laju pencorakan) serta proses punaran dikawal dengan baik.

Kata kunci: Corak berskala nano; litografi AFM; nanowayar silikon; peranti nano

INTRODUCTION

Extensive researches have been done in order to produce various nanostructured materials such as nanowires, nanorods, quantum dots and nanoparticles. Silicon nanowire (SiNW) is one of the promising nanostructures in the development of nanodevices. Moreover, SiNW is compatible with complementary metal-oxide semiconductor (CMOS) technology; it is a very attractive material to be used as interconnection materials and basic components for nanoelectronic and optoelectronic with lower power consumption such as light emitting diode (LED) and high speed field effect transistor (FET) (Rosoft 2002).

SiNW based devices can be fabricated by top-down and bottoms-up approach such as chemical-vapour-deposition (CVD) (Lee et al. 2009; Salem et al. 2009; Suk et al. 2008; Yoon et al. 2008), electron beam lithography and laser induced decomposition (Salem et al. 2009). These techniques are very complex and require expensive masking system. Therefore, in this research, an alternative technique which is AFM lithography has been developed for the fabrication of SiNW based devices.

There are two types of the scanning probe microscopes (SPMs) which are scanning tunneling microscope (STM) and atomic force microscope (AFM). The STM is a useful tool to characterize the surface structures for conducting

materials. Due to the data from the STM images that provides information on the relative importance of molecule-molecule and molecule-substrate interaction, it is useful in such applications as microelectronic fabrication, epitaxial growth of thin films, lubrication and chromatography. Meanwhile, the AFM was developed to characterize the surface structures for non-conducting as well as for conducting materials. The AFM is mostly used to characterize the surface of the thin film, polymer coating and single-crystal substrates.

The AFM lithography works based on the principle of interaction between the probe and substrate separation in close contact condition ~1 nm. Therefore, the AFM lithography can operate in contact mode (Fu et al. 1999; Giesbers et al. 2008; Hu & Hu 2005; Kuramochi et al. 2003, 2004; Park et al. 2007) or noncontact mode (Fang 2004; Fang et al. 2008; Hsu & Lee 2008; Hutagalung et al. 2007; Kuramochi et al. 2004). When suitable external field applied and/or forces are exerted, the probe can induce various physical and chemical processes on the substrate surface. Due to the physical and chemical processes on the substrate surface, the localized nanostructures are generated.

AFM lithography possesses the versatility to pattern a wide range of materials including metals, semiconductors, polymers and biological molecules in different media. The surface topography and physical properties of the fabricated localized nanostructures can be immediately characterized with AFM (Xie et al. 2006). As usual, the AFM is used as a microscope to directly illustrate the image on the surface topography with atomic and molecular resolution. The image of the surface is obtained by recording and regulating the force felt by a probe as it scans the surface.

AFM lithography can be classified into two groups in term of their operational principles which are bias-assisted AFM lithography and force-assisted AFM lithography. In bias-assisted AFM lithography (as used in this project), the AFM tip is biased to create a localized electric field and the AFM tip acts as a nanoscale electrode for current injection or collection. Depending on the magnitude of the tip's bias (positive bias or negative bias) and substrate materials, the application of the tip voltage can lead to anodic oxidation for nanostructures, nano-lines or nano-dots fabrication (Xie et al. 2006).

In force-assisted AFM lithography, a large force is applied to the tip for pattern fabrication and the tip - surface interaction is mainly mechanical. During force-assisted AFM lithography, forces larger than those used for AFM imaging are loaded onto the tip. The initially featureless surface is then patterned by mechanically scratching, pushing or pulling the surface atoms and molecules with the probe (Xie et al. 2006). Park et al. (2007) had used force-assisted AFM lithography for the formation of the damage layer on silicon substrate by a simple scratching process using special designed diamond tip cantilever for industrial application as a micro-to-nano machining tool.

In this work, a SiNW based device namely silicon nanowire transistor (SiNWT) was developed using a nanowire as a channel that is in contact with the source (S), drain (D) and very close to gate (G). The SiNWT was fabricated by AFM lithography and followed by wet chemical etching processes. AFM lithography was performed by local anodic oxidation (LAO) process. The oxide patterns grew on the chemically reactive substrate which acts as a mask by the application of a voltage between a conductive AFM tip and its substrate. There are several parameters that influence the patterning process such as tip writing speed, relative air humidity, sample voltage tip, radius tip, sample distance tip, anodization time and crystalline orientation.

The AFM lithography can only produce SiNWT structures formed as the oxide pattern mask. TMAH and HF can be chosen for silicon and silicon oxide etching. TMAH is an anisotropic chemical etchant and CMOS compatible, it was used to remove the uncovered silicon layer and leave behind the oxide pattern. Meanwhile, HF acid was used to remove oxide layer.

METHODS

The materials used in the SiNWT fabrication are silicon on insulator (SOI) wafer, de-ionized (DI) water, hydrogen peroxide (H_2O_2), hydrofluoric acid (HF), hydrochloric acid (HCI), ammonium hydroxide (NH_4OH) and tetramethylammonium hydroxide (TMAH). These materials have their own function. The SOI wafer has three layers; silicon (100 nm) on the top layer followed by the buried oxide layer (BOX, 200 nm) as insulator and the bottom layer of silicon substrate (6.25 μm). The p-type SOI wafer with six inch in diameter, <100> orientation and resistivity of 14-22 Ωcm was supplied by SOITEC. TMAH is an anisotropic etchant of silicon which is a colourless solution, less harmful, CMOS compatible, smooth, non-flammable and high etching selectivity to silicon.

The SiNWT was fabricated on pre-cleaned SOI wafer. A pre-designed of the SiNWT patterns was drawn as a very thin oxide layer on the SOI surface by AFM lithography technique. After that, the patterns etched by TMAH (25 wt. %) and HF (2 wt. %) to remove the unwanted silicon layer and oxide layer, respectively (Hutagalung & Lew 2011, 2012; Lew & Hutagalung 2010).

SiNWT structures were designed by using a Nanonavi vector scan programme which installed in scanning probe microscope (SPM) (SPI3800N/4000) machine. The lithography process is performed by using conductive AFM mode operated in non-contact mode. The nanoscale oxide pattern of SiNWT structures is drawn using an overall gold coating tip by applying 7 to 9 V voltage to the tip under controlled humidity and tip writing speed of 6 μm/s. The SiNWT patterns were etched by immersing the sample in a container that contained 25 wt. % TMAH solution with the etching time range of 30 s at 65°C. In order to produce the SiNWT, the sample was etched by 2 wt. % HF for 5 s to remove the oxide capped of the SiNWT pattern.

Finally, the fabricated SiNWT characterized by AFM, FESEM and EDX. AFM was used to characterize the topography and dimension of the devices. FESEM and EDX were used for the surface morphology, dimension and elemental composition of the fabricated devices. The overall process flow chart and schematic diagram of the SiNWT fabrication are shown in Figure 1.

Results and Discussion

The nanoscale oxide patterning process is performed by applied voltage to the AFM tip of 7, 8 and 9 V under 6 μm/s tip writing speed. During patterning, generated electric field between the tip and sample surface will promote formation of thin oxide layer on surface (Cervenka et al. 2006; Fang 2004; Gwo 2001; Held et al. 1998; Xie et al. 2006). In this research, the generated electric field was in the range of $7 - 9 \times 10^9$ V/m by applying tip voltage of 7-9 V. Figure 2 shows the two- and three-dimensional AFM images of device structures before and after AFM lithography process at various tip applied voltages with tip writing speed of 6 mm/s. The images show that the pre-designed nanoscale oxide patterns have been successfully fabricated at 7 V applied voltage (Figure 2(b)). From topography

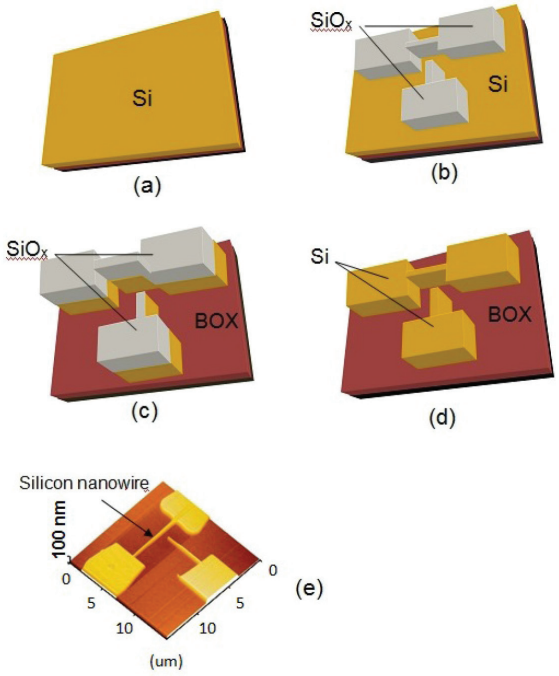

FIGURE 1. Schematic diagram of the SiNWT fabrication (a) p-type silicon-on-insulator (SOI) wafer, (b) nanoscale oxide patterning by AFM, (c) etched with 25 wt. % TMAH in water solution, (d) etched with 2 wt. % HF and (e) typical produced silicon nanowire transistor (SiNWT)

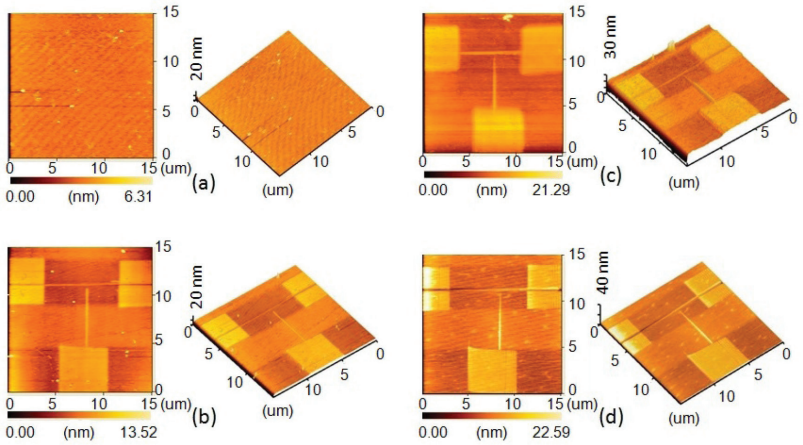

FIGURE 2. Effect of applied voltage to AFM tip on the formation of nanostructure patterns at writing speed of 6 μm/s (a) before patterning, (b) 7 V, (c) 8 V and (d) 9 V

analysis of the sample surface obtained that the colour contour in the AFM images is increased when the applied tip voltage increased. This indicated that the thickness of the pre-designed nanoscale oxide pattern of device structure is increased due to the increment of applied tip voltages. Therefore, it is well justified that the tip voltage will influence the formation of oxide patterns by AFM lithography. In the current study, it was shown that 7 V tip voltage with 6 µm/s tip writing speed is an acceptable condition for nanodevice structures patterning.

Figure 3 shows the effect of oxide thickness patterned by tip voltage from 7-9 V at tip writing speed of 6 µm/s. From the measurement, the thickness of oxide pattern is increased linearly due to the increasing of tip voltage.

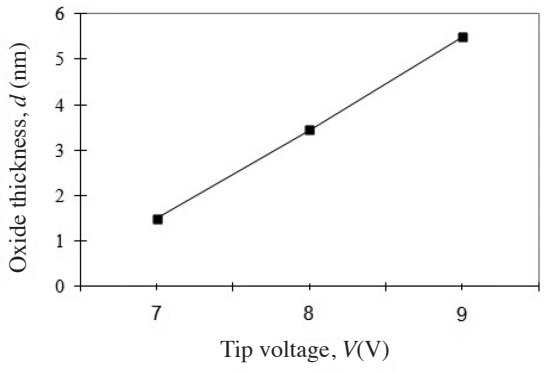

FIGURE 3. Graph of grown oxide thickness versus applied tip voltage

After lithography process, the patterned structures etched by TMAH (25 wt. %) to remove unwanted silicon layer. From previous studies, silicon etching process is commonly done by KOH or TMAH solution (Nguyen & Elwenspoek 2006). In this research, TMAH etchant was used to remove the uncovered 100 nm silicon layer of SOI wafer and to remain the nanoscale oxide patterns in which the buried oxide layer is acted as etch stop.

Figure 4 shows the AFM images of device structures after nanoscale oxide patterning and etched with 25 wt. % TMAH in water solution at 65°C for 30 s. From the two-dimensional AFM image in Figure 4, the contour colour of fabricated device after etched by TMAH is higher compared with the images of patterned structures before etching process. When device etched with TMAH for 30 s, the contour colour became 102.06 nm compare to 13.52 nm before the etching process. This proved that the uncovered silicon layer by the nanoscale oxide pattern had been etched away by the TMAH.

In order to produce a complete device (SiNWT), the oxide pattern which acted as a mask during TMAH etching process has to be removed by using HF (Williams & Muller 1996). The nanoscale oxide patterns can be removed by immersing the device in 1:20 solution of HF:DI water for 5 s. Figure 5 shows the AFM images of device (SiNWT) after etched with 25 wt. % TMAH in water solution at 65°C for

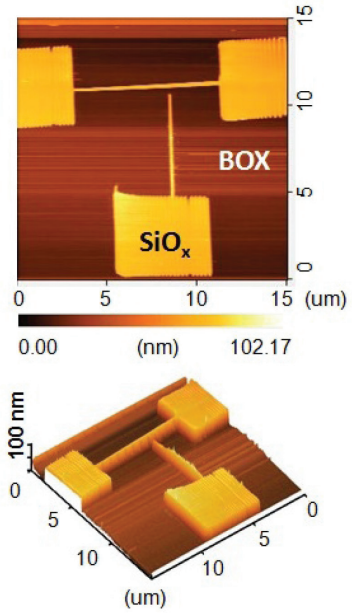

FIGURE 4. Two-and three-dimensional AFM images of patterned devices after etched with TMAH

30 s and subsequently etched with 1:20 solution of HF:DI water for 5 s.

The fabricated device (SiNWT) was characterized by EDX after silicon oxide etching process with HF solution. From the EDX analysis, oxygen and silicon elements were observed on device (nanowire and pads) and substrate (BOX of SOI wafer) after the HF etching process. Figure 6 shows the EDX results obtained from selected point on both device's pad and substrate. The pad contained 27.10

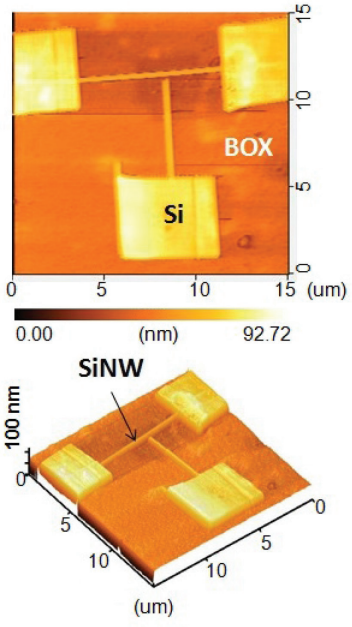

FIGURE 5. AFM images of device (SiNWT) after etched with TMAH and subsequently etched with 1:20 solution of HF:DI water for 5 s

at. % element of oxygen and 72.90 at. % element of silicon (Figure 6(a)) compared to 51.55 at. % element of oxygen and 48.45 at. % element of silicon on substrate (BOX SOI wafer) (Figure 6(b)). Silicon is dominant element in the device's pad of the fabricated SiNWT, while oxygen content dominant in the substrate. This proved that SiNW based device has been successfully fabricated.

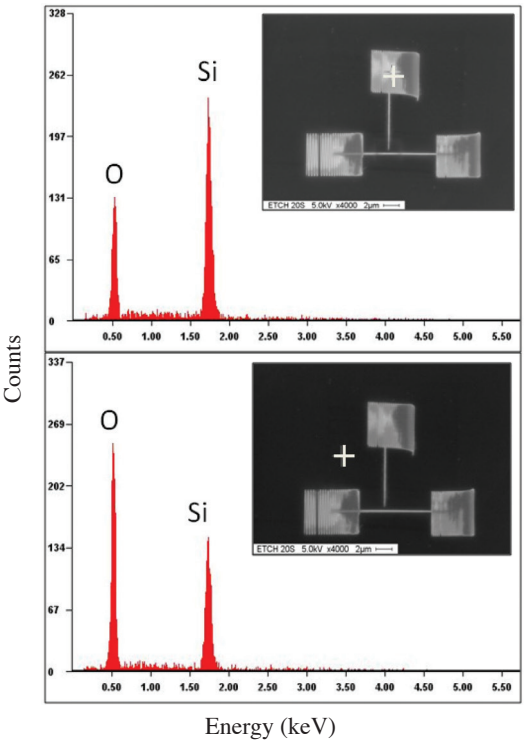

FIGURE 6. Elemental analysis of fabricated device (SiNWT) structures (a) pad and (b) substrate

CONCLUSION

AFM lithography followed by the wet chemical etching processes can be utilized for the fabrication of nanodevice structures such as SiNWT. For SiNWT fabrication the involved steps are cleaning of SOI substrate followed by patterning of device structure on the SOI surface by AFM lithography via LAO and two steps etching processes (TMAH and HF etching). By well controlling the lithography process (applied tip voltage and writing speed) as well as the etching processes, a various structures of nanodevices can be fabricated.

ACKNOWLEDGEMENTS

This work is supported by Research University Grant (RUI), Universiti Sains Malaysia under project number 1001/PBAHAN/814167.

REFERENCES

Cervenka, J., Kalousek, R., Bartos, M., Skoda, D., Tomanec, O. & Sikola, T. 2006. Fabrication of nanostructures on Si(100) and GaAs(100) by local anodic oxidation. *Applied Surface Science* 253: 2373-2378.

Fang, T-H., Wang, T.H. & Wu, K-T. 2008. Local oxidation of titanium films by non-contact atomic force microscopy. *Microelectronic Engineering* 85: 1616-1623.

Fang, T-H. 2004. Mechanisms of nanooxidation of Si(100) from atomic force microscopy. *Microelectronics Journal* 35: 701-707.

Fu, E.S., Wang, X-S. & Williams, E.D. 1999. Characterization of structures fabricated by atomic force microscope lithography. *Surface Science* 438: 58-67.

Giesbers, A.J.M., Zeitler, U., Neubeck, S., Freitag, F., Novoselov, K.S. & Maan, J.C. 2008. Nanolithography and manipulation of graphene using an atomic force microscope. *Solid State Communications* 147: 366-369.

Gwo, S. 2001. Scanning probe oxidation of Si_3N_4 masks for nanoscale lithography, micromachining, and selective epitaxial growth on silicon. *Journal of Physics and Chemistry of Solids* 62: 1673-1687.

Held, R., Heinzel, T., Studerus, P. & Ensslin, K. 1998. Nanolithography by local anodic oxidation of metal films using an atomic force microscope. *Physica E: Low-dimensional Systems and Nanostructures* 2: 748-752.

Hsu, H-F. & Lee, C-W. 2008. Effects of humidity on nano-oxidation of silicon nitride thin film. *Ultramicroscopy* 108: 1076-1080.

Hu, X. & Hu, X. 2005. Analysis of the process of anodization with AFM. *Ultramicroscopy* 105: 57-61.

Hutagalung, S.D., Darsono, T., Yaacob, K.A. & Ahmad, Z.A. 2007. Effects of tip voltage and writing speed on the formation of silicon oxide nanodots patterned by scanning probe lithography. *Journal of Scanning Probe Microscopy* 2: 28-31.

Hutagalung, S.D. & Lew, K.C. 2011. Current-voltage characteristics of side-gated silicon nanowire transistor fabricated by AFM lithography. *Advanced Materials Research* 277: 84-89.

Hutagalung, S.D. & Lew, K.C. 2012. Effect of TMAH etching duration on the formation of silicon nanowire transistor patterned by AFM nanolithography. *Sains Malaysiana* 41: 1023-1028.

Kuramochi, H., Ando, K. & Yokoyama, H. 2003. Effect of humidity on nano-oxidation of p-Si(001) surface. *Surface Science* 542: 56-63.

Kuramochi, H., Ando, K., Tokizaki, T., Yasutake, M., Perez-Murano, F., Dagata, J.A. & Yokoyama, H. 2004. Large scale high precision nano-oxidation using an atomic force microscope. *Surface Science* 566-568: 343-348.

Lee, S.K., Lee, S.Y., Rogdakis, K., Jang, C.O., Kim, D.J., Bano, E. & Zekentes, K. 2009. Si nanowire p-FET with asymmetric source-drain I-V characteristics. *Solid State Communications* 149: 461-463.

Lew, K.C. & Hutagalung, S.D. 2010. Silicon nanowire transistor fabricated by AFM nanolithography followed by wet chemical etching process. *International Journal of Nanoscience* 9: 289-293.

Nguyen, Q.D. & Elwenspoek, M. 2006. Characterisation of anisotropic etching in KOH using network etch rate function model: Influence of an applied potential in terms of microscopic properties. *Journal of Physics: Conference Series* 34: 1038-1043.

Park, J.W., Lee, S.S., So, B.S., Jung, Y.H., Kawasegi, N., Morita, N. & Lee, D.W. 2007. Characteristics of mask layer on (100)

silicon induced by tribo-nanolithography with diamond tip cantilevers based on AFM. *Journal of Materials Processing Technology* 187-188: 321-325.

Rosoft, M. 2002. *Nano-Surface Chemistry*. New York: Marcel Dekker, Inc.

Salem, B., Dhalluin, F., Abed, H., Baron, T., Gentile, P., Pauc, N. & Ferret, P. 2009. Self-connected horizontal silicon nanowire field effect transistor. *Solid State Communications* 149: 799-801.

Suk, S.D., Yeo, K.H., Cho, K.H., Li, M., Yeoh, Y.Y., Lee, S.Y., Kim, S.M., Yoon, E.J., Kim, M.S., Oh, C.W., Kim, S.H., Kim, D.W. & Park, D. 2008. High-performance twin silicon nanowire MOSFET (TSNWFET) on bulk Si wafer. *IEEE Transactions on Nanotechnology* 7: 181-184.

Williams, K.R. & Muller, R.S. 1996. Etch rates for micromachining processing. *Journal of Microelectromechanical Systems* 5: 256-269.

Xie, X.N., Chung, H.J., Sow, C.H. & Wee, A.T.S. 2006. Nanoscale materials patterning and engineering by atomic force microscopy nanolithography. *Materials Science and Engineering: R: Reports* 54: 1-48.

Yoon, C., Kang, J., Yeom, D., Jeong, D.Y. & Kim, S. 2008. Comparison of electrical characteristics of back- and top-gate Si nanowire field-effect transistors. *Solid State Communications* 148: 293-296.

Sabar D. Hutagalung*, Kam Chung Low & Teguh Darsono
School of Materials and Mineral Resources Engineering
Engineering Campus, Universiti Sains Malaysia
14300 Nibong Tebal, Penang
Malaysia

Sabar D. Hutagalung*
Physics Department
Faculty of Science
Jazan University, Jazan
Saudi Arabia

*Corresponding author; email: mrsabar@eng.usm.my

Received: 7 January 2013
Accepted: 19 July 2013